REMARKS

Claims 1-19 are now pending in the application. Claims 1, 9 and 12 have been cancelled. New Claims 17-19 are presented fro consideration. The Examiner is respectfully requested to reconsider and withdraw the rejection(s) in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 103

Claims stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Murty (U.S. Pat. No. 4,544,868) in view of Heinkel et al. (U.S. Pat. No. 6,351,091). This rejection is respectfully traversed.

Applicants believe that the original claims 1, 9 and 12 set forth sharing of a fixed DC current level in sufficient detail to delineate over the prior art of record. In the interest of expediting prosecution, Applicants are presenting new claims 17-19, which more particularly define sharing of a fixed DC current level.

The present invention regulates the DC bus current to a fixed current level. In one embodiment, pulse width modulation is used to regulate the DC bus current to the fixed current level although other methods can be used. In the example set forth in the specification, the fixed bus current is 1mA. Initially the current in the first phase is 1 mA before the overlap period starts. After the overlap period starts, the current in the first phase is reduced to 0.9 mA and the current in the second or next phase is increased to 0.1 mA. The decreasing/increasing current distribution trend continues to 0.8mA/0.2mA, 0.7mA/0.3mA, etc until the overlap period ends when the second phase receives the entire fixed current level (1mA). As can be appreciated, other current

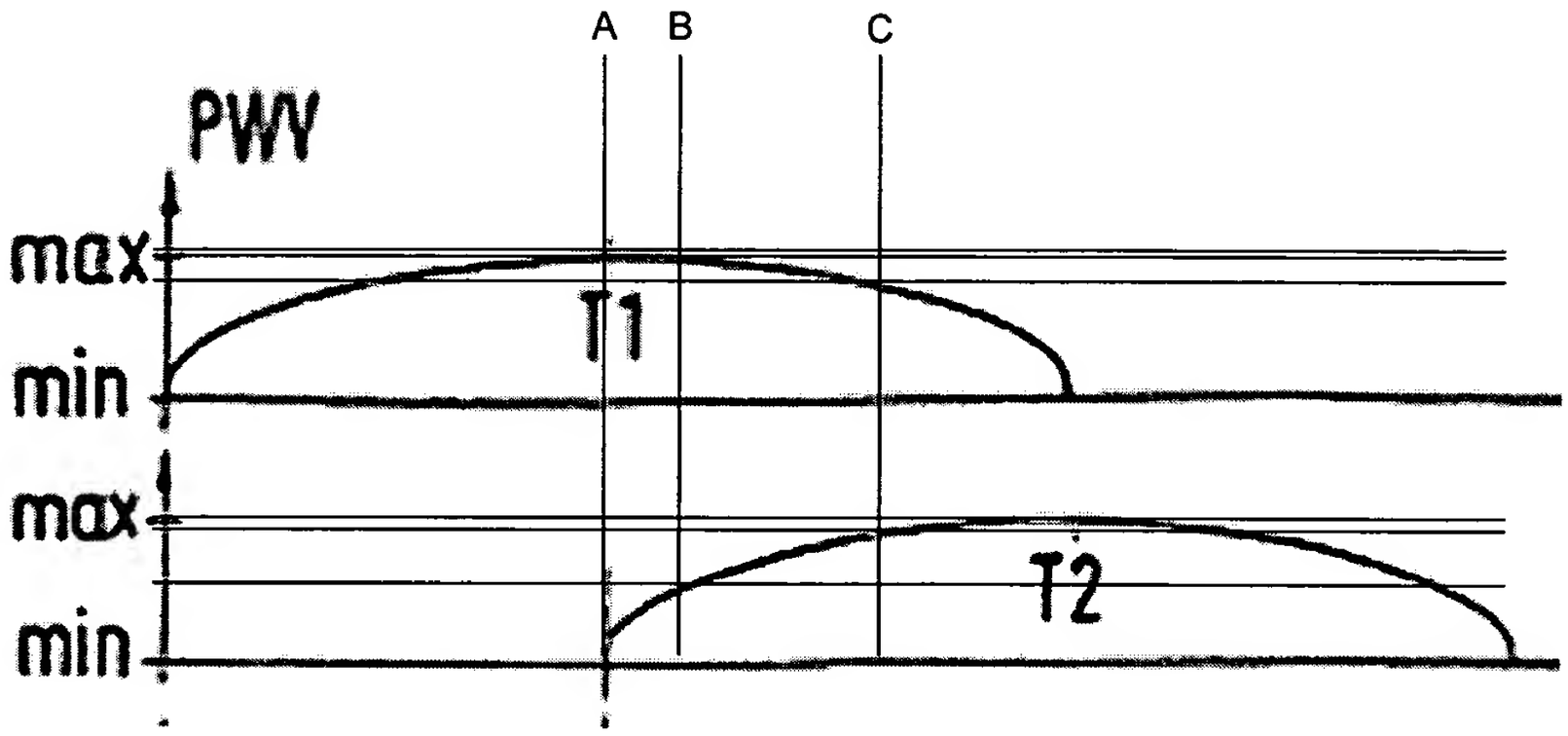
values can be used. The transition may be linear or nonlinear as long as the total current is shared (e.g. remains equal to the fixed DC current level).

Regarding new Claims 17, 18 and 19, Murty does not show teach or suggest a switching circuit, method or control module that forces current sharing by decreasing the DC bus current to one phase while increasing the DC bus current to a subsequent phase. As has been admitted by the Examiner, there is no overlap in Murty. One phase starts when the prior phase ends.

Heinkel et al. does not show teach or suggest a switching circuit, method or control module that decreases the DC bus current to one phase while increasing the DC bus current to a subsequent phase such that the fixed current level is shared and such that a sum of the current to first and second phases is substantially equal to the fixed current level.

The current that is provided to the phases is pulse width modulated in Heinkel et al. Heinkel et al. is completely silent on the issue of the sum of the current from the prior phase and the next phase during overlapping periods. As can be seen in FIG. 4 of Heinkel et al. set forth below, the two phases do not share the DC bus current as claimed such that the sum is equal to a fixed DC current level. The overlap period starts at time A. At time B, the PWM ratio or duty cycle of the first phase is approximately 95% and the PWM ratio or duty cycle of the second phase is approximately 50%. Therefore, at time B the current at the first phase is approximately 0.95mA (assuming a maximum 1mA first phase current) and the current at the second phase is approximately 0.5mA (assuming a maximum 1mA second phase current supply). At time C, the PWM ratio or duty cycle of the first phase is approximately 85%

(or 0.85mA) and the PWM ratio or duty cycle of the second phase is approximately 90-95% (or 0.9mA).



There does not appear to be any relationship between the current in the phases during the overlapping periods relative to a fixed DC level as set forth in the Claims 17-19.

Based on the foregoing, Applicants believe that Claims 17-19 are allowable over the prior art of record. The remaining claims are either directly or indirectly dependent upon Claims 17-19 and are allowable for the same reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt

and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1211.

Respectfully submitted,

Dated: June 16, 2003

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